Amendments to the Specification:

Please replace the paragraph that begins on page 4, line 8 with the following paragraph:

Figure 1 shows a block diagram of a system 100 which includes a typical interface between two data communication components such as a synchronous optical network (SONET) framer 110 and a serialization-deserialization (SERDES) device 150. As shown in Figure 1, data can be transmitted from the SONET framer 110 to the SERDES device 150 via the data path TXDATA 112. In this example, the TXDATA is 16-bit wide in parallel mode. The TXCLK signal 114 is the source synchronous clock for ~~TXDADA~~ TXDATA and the TXCLK_SRC 116 is the reference clock from the SERDES device 150 to the SONET framer 110. Data can be transmitted from the SERDES device 150 to the SONET framer 110 via the data path RXDATA 152. In this example, the RXDATA is also 16-bit wide in parallel mode. The RXCLK 154 is a clock signal for RXDATA. In this example, the REFCLK 130 is a reference clock signal at the board level.

Please replace the paragraph that begins on page 4, line 25 with the following paragraph:

Figure 2 illustrates a more detailed block diagram of a system 200 including a typical interface between two data communication devices (e.g., a SONET framer and a SERDES device). In this configuration, data are transmitted from the SONET device 210 to the SERDES device 250 via the data path ~~TXDADA~~ TXDATA 212 which, in this example, is 16-bit wide. The RXDATA which is also 16-bit wide in this example is used for data transmission from the SERDES device 250 to the SONET framer 210. The TXCLK 214 is a source synchronous clock signal for TXDATA. The TXCLK_SRC 216 is a reference clock signal from the SERDES device 250 to the SONET framer 210. Delay variations in the round trip delay of the transmit data path (TXCLK_SRC to TXCLK) are accommodated using the clock synthesis unit 260 and the PFC unit 270. However, this only ~~account~~ accounts for variations of one of the signals of a parallel bus, TXCLK in this example. This kind of delay adjustment is also called parallel delay adjustment herein. However, delay variations of individual bits are not accommodated or provided for the traditional systems or methods of data communications.

Please replace the paragraph that begins on page 5, line 20 with the following paragraph:

Figure 3 shows a block diagram of one embodiment of a data communication apparatus/system 300 according to the teachings of the present invention. The system 300 as shown in Figure 3 includes a first device 310 and a second device 320 that are configured to transfer data to each other. In one embodiment, the first device 310 is configured as a transmitter device and the second device 320 is configured as a receiver device. As an example, a transmitter device can be a SONET framer and a receiver device can be a SERDES device. It should be understood and appreciated by one skilled in the art that the teachings of the present invention are applicable to any system, apparatus, or method for data communication between two devices or components including those devices and components in optical networking technologies. In one embodiment, the first device 310 transmits data to the second device 320 in parallel mode via a parallel bus 330. For example, the first device 310 may be configured to transmit data to the second device 320 in form of data words with each data word containing a plurality of data bits (e.g., 8 bits, 16 bits, 32 bits, etc.). As shown in Figure 3, the first device or transmitter 310 includes a circuit called bit phase alignment circuit 312 and a circuit called bit position alignment circuit 314. The second device or receiver 320 includes a circuit called bit phase detect circuit 322 and a circuit called bit position sampler circuit 324. In one embodiment, the bit phase detect circuit 324 is configured to individually detect the phase of each data bit against a companion parallel clock called UNLOAD_CKP 332. In one embodiment, the bit phase detect circuit 324 is configured to feed back the phase information detected with respect to the individual data bits to the first device or transmitter 310 via a signal path 334 (called UNLOAD_PHASE herein). In one embodiment, the bit phase detect circuit 324 serially feeds back the phase information to the corresponding bit phase alignment circuit 312. In one embodiment, the bit phase alignment circuit 312 is configured to individually ~~adjusts~~ adjust the output delay of each data bit being transmitted over the parallel bus 330, based upon the phase information received from the bit phase detect circuit ~~324~~ 322. Thus, delay variations with respect to each individual data bit due to variations in distance between individual bits of the parallel data bus 330 can be adjusted or accommodated accordingly. In one embodiment, the bit position alignment circuit 314 is configured to transmit parallel data patterns (also called data samples or simply samples herein) to the bit position sampler circuit 324 in the second device 320, via a signal path 336 (called SAMPLE herein). In one embodiment, the bit position sampler

circuit samples and holds the parallel data patterns received from the bit position alignment circuit 314, in response to a request or order by the bit position alignment circuit 314. In one embodiment, the bit position sampler circuit 324, after sampling the data patterns, feeds back the sampled data to the bit position alignment circuit 314 via a signal path 340 (called UNLOAD_DATA herein). In one embodiment, the sampled data can be fed back serially from the bit position sampler circuit 324 to the bit position alignment circuit 314. In one embodiment, upon detecting or recognizing phase variations that are in excess of one bit of the sampled data fed back from the bit position sampler circuit 324, the bit position alignment circuit 314 individually shifts data bit positions between parallel data words to align phase variations that are in excess of one bit interval. Accordingly, phase variations in excess of one bit interval are also adjusted.